

Claims

1-7. (cancelled)

8. (Currently amended) A method for actuating function units (FUs) in a processor, wherein a configuration phase involves a series of primary instruction words that come from a translation of a program code being divided into a series of instruction word parts, with a program cycle involving instruction words which actuate the processor being constructed in the full instruction word length to form a Very Long Instruction Word (VLIW) ~~VLIW~~ and being buffer-stored in an instruction word memory (cache), the method comprising:

a first step that involves a primary instruction word being divided, in the configuration phase, into the series of a particular number of instruction word parts which are used for constructing a respective VLIW during the execution phase, with a respective first and second ~~FIW (Function Instruction Word part)~~, Function Instruction Word (FIW) part, being preceded with an associated first or second operating code, which thus determines how the cache's memory location taken up by the respective FIW is handled in the execution phase,

wherein the respective first and second operating code are respectively followed by an associated first and second tag that represent the information regarding which of ~~the a~~ first and ~~the a~~ second FU actuates the respective FIW,

wherein the respective first and second operating code and their associated first or second tag are combined with the respective first and second FIWs to form the first

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and second Tagged Very Long Instruction Word (TVLIW) TVLIW containers all of which represent the TVLIW; and

a second step that involves the respective available TVLIW being converted into an Headed Very Long Instruction Word (HVLIW) HVLIW in the configuration phase, wherein the HVLIW contains a preceding general header, and wherein the HVLIW with its code-compressed structure replaces all functions of the TVLIW; and

a third step that involves, in an execution phase, executing the HVLIW with its code-compressed structure to actuate the functioning units (FUs) in the processor, wherein a Command Code mode of operation of the HVLIW and its associated general header is implemented so that the general header is followed directly by the first and second FIWs required for constructing the VLIW (22), wherein the general header stores the information in coded form, which indicates all combinations regarding which of the first and second FIW (instruction word part) is provided, after decoding in the execution phase for actuating a respective first and/or second FU (function unit) in the processor, and wherein the general header stores which first and/ or second FIW take up memory locations in a cache and whether or which operations are to be executed with the respective memory content in the execution phase in the cache when constructing the VLIW.

9. (Cancelled)

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10. (Currently amended) The method of ~~claim 4~~ claim 8 wherein a first part of the general header is provided with a header mode that contains information about the “Command Code” mode of operation of the HVLIW and of the general header, wherein the first part is followed by a second part that stores, coded as table values, the respective most needed combination regarding which of the respective FUs is actuated by which of the first and second FIW, wherein a third part is connected as CE information and contains a pointer which refers to a provided location in a dictionary, and wherein the last part of the general header provided is the supplementary information.

11. (Currently amended) The method of ~~claim 4~~ claim 8 wherein a “reference instruction” mode of operation of the HVLIW and of the contained general header is implemented in which the FIWs provided for constructing the VLIW in the execution phase are buffer-stored in the cache, wherein the associated header mode bears a correspondingly decodable tag for this “reference instruction” mode of operation,

wherein the “reference instruction” mode of operation is initiated by a specific HVLIW that contains an address statement which is used to refer to a reference instruction,

wherein the subsequent HVLIW which likewise bears the tag for the “reference instruction” mode of operation, contains a relative address for the address statement provided by the reference, and

wherein a mask appended to it for the FUs which are to be excluded from the actuation.

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12. (Currently amended) The method of ~~claim 4~~ claim 11 wherein the address statement of the specific HVLIW which initiates the “reference instruction” mode of operation refers to a general address.

13. (Currently amended) The method of ~~claim 4~~ claim 8 wherein the execution phase involves the HVLIW being decoded in a decoder which is equipped with a header decoder, a CMDT, a cache and a cache miss repair logic unit, wherein the HVLIW is buffer-stored in the cache, and wherein the header decoder identifies the mode of operation of the general header from the header mode stored therein,

wherein the identified header mode is taken as a basis for decompressing the values of the FU-C information which are provided in the general header by means of a comparison with the CMDT and in conjunction with the CE information which is likewise taken from the general header,

wherein the identified header mode is taken as a basis for processing the supplementary information in the general header, and

wherein possible incorrect access during buffer-storage in the cache (cache miss) is remedied by the execution of an error handling routine in a cache miss repair logic unit and a valid VLIW is provided at the output of the decoder.